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WPI Acc No: 1990-212441/199028

XRAM Acc No: C90-091705

XRPX Acc No: N90-165028

**Anodic bonding of silicon wafer and glass substrate - by
heating after contacting with cathode plate and applying DC voltage**

Patent Assignee: MITSUBISHI DENKI KK (MITQ)

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2141442	A	19900530	JP 88293956	A	19881121	199028 B
JP 95112939	B2	19951206	JP 88293956	A	19881121	199602

Priority Applications (No Type Date): JP 88293956 A 19881121

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 95112939	B2		3	C03C-027/00	Based on patent JP 2141442

Abstract (Basic): JP 2141442 A

Si-wafer and glass substrate are bonded anodically by abutting a Si-wafer on the main surface of a glass substrate, abutting a cathode conductor plate on the other main surface - e, applying dc voltage with the Si-wafer, as an anode, and the cathode conductor plate, as a cathode, for heating them simultaneously. The abutting location of the cathode conductor on the glass substrate is set at a location opposite to the outer periphery of the Si-wafer, then the voltage is applied to achieve the bonding.

USE/ADVANTAGE - Useful in semiconductor devices, reducing residual stress at the interface between Si-wafer and glass substrate, and obtg. uniform distribution of residual stress at the in-plane of the wafer.

(5pp Dwg.No.1,3/5) 2

Title Terms: ANODE; BOND; SILICON; WAFER; GLASS; SUBSTRATE; HEAT; AFTER;
CONTACT; CATHODE; PLATE; APPLY; DC; VOLTAGE

Derwent Class: L03; U11

International Patent Class (Main): C03C-027/00

International Patent Class (Additional): H01L-021/52; H01L-029/84

File Segment: CPI; EPI

Manual Codes (CPI/A-N): L04-C17; L04-C22

Manual Codes (EPI/S-X): U11-D03B3; U11-E02A3

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